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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/534,170	05/05/2005	Keiji Mabuchi	09792909-6249	9957

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EXAMINER	
HSU, AMY R	

ART UNIT	PAPER NUMBER
2622	

MAIL DATE	DELIVERY MODE
11/12/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/534,170	MABUCHI, KEIJI	
	Examiner	Art Unit	
	AMY HSU	2622	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 July 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4 and 6-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4 and 6-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *8/8/08*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. Applicant's request for reconsideration of the finality of the rejection of the last Office action is persuasive and, therefore, the finality of that action is withdrawn.

Response to Arguments

2. Applicant's arguments, filed 7/23/2008, with respect to the rejection(s) of claim(s) 1-11 under 35 U.S.C. 103(a) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of further relevant prior art findings.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-3,6 ,8-11 are rejected under 35 U.S.C. 102(b) as being anticipated by ISSCC 2001/ SESSION 6/ CMOS IMAGE SENSORS WITH EMBEDDED PROCESSORS/ 6.1: A 10kframe/s 0.18μm CMOS Digital Pixel Sensor with Pixel-Level Memory, hereinafter referred to as "Pixel-Level Memory".

Regarding Claim 1, Pixel-Level Memory teaches a solid-state imaging apparatus comprising: a pixel array, said pixel array comprising a plurality of pixels in a two-dimensional array (*Fig. 6.1.7)*; a pixel-array scanning circuit that scans the pixel array to

read analog signals from the individual pixels to an AD (analog to digital) memory (*Fig. 6.1.1, and paragraph 5 teach the analog signals are scanned and read, "A/D conversion...after…charge transfer", to the A/D converter to the pixel level memory, and there is circuitry to enable this)*, the AD memory comprising a plurality of unit memories in a two-dimensional array corresponding to a pixel arrangement in the pixel array for storing said analog signals, each unit memory including an analog to digital converter circuit (*paragraph 1 teaches each pixel has an ADC and paragraph 8 teaches each pixel also has a corresponding memory)*, and each said analog to digital converter circuit producing a converted digital signal by carrying out analog to digital conversion on a stored analog signal (*this is inherent of analog to digital converter circuits)*; and a memory scanning circuit for scanning the AD memory and outputting the converted digital signals from the individual unit memories (*paragraph 7 teaches pixel values are read out of memory)*.

Regarding Claim 2, Pixel-Level Memory teaches the solid-state imaging apparatus according to claim 1, further comprising an output unit that processes the digital signals output from the memory scanning circuit and outputs the processed signals out of the apparatus. Paragraph 3 teaches the output periphery.

Regarding Claim 3, Pixel-Level Memory teaches the solid-state imaging apparatus according to claim 1, wherein the individual pixels in the pixel array correspond to the individual unit memories in the AD memory in a one- to-one

relationship. Paragraph 8 teaches each pixel has a unit memory.

Regarding Claim 6, Pixel-Level Memory teaches the solid-state imaging apparatus according to claim 1, wherein AD conversion is simultaneously carried out for all the unit memories in the AD memory. Paragraph 1 teaches all ADCs operate in parallel.

Regarding Claim 8, Pixel-Level Memory teaches the solid-state imaging apparatus according to claim 1, wherein the unit memories comprise DRAMs. Paragraph 8 teaches the memories are DRAM.

Regarding Claim 9, Pixel-Level Memory teaches a solid-state imaging apparatus comprising: a pixel array, said pixel array comprising a plurality of pixels in a two-dimensional array (*Fig. 6.1.7)*; and an AD (analog to digital) memory for storing analog signals read from the pixel array and carrying out AD conversion on said analog signals, the AD memory comprising a plurality of unit memories in at least a two-dimensional array corresponding to a pixel arrangement in the pixel array, each unit memory including an analog to digital converter circuit (*paragraphs 1,5 and 8)*, and the plurality of unit memories carrying out AD conversion on signals from at least two rows of pixels simultaneously (*paragraph 1 ADCs operate in parallel).*

Regarding Claim 10, Pixel-Level Memory teaches the solid-state imaging apparatus according to claim 9, wherein the plurality of unit memories simultaneously AD convert signals that are obtained by combining signals read from the pixel array (*paragraph 1 ADCs operate in parallel)*.

Regarding Claim 11, Pixel-Level Memory teaches the solid-state imaging apparatus according to claim 9, wherein the unit memories carry out noise removal and on AD convert the signals from the pixel array. Paragraph 1 teaches this structure reduces or eliminates noise.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Pixel-Level Memory in view of Gowda et al. (US 6275259).

Regarding Claim 4, Pixel-Level Memory teaches the solid-state imaging apparatus according to claim 1, and teaches each pixel contains and therefore corresponds with one AD memory, but does not teach N pixels to one AD memory, wherein N>2. Pixel-Level Memory teaches that each pixel has an ADC and a memory;

therefore it is taught that an ADC corresponds to a memory. One of ordinary skill in the art would realize that sharing one memory structure between two or more pixel would save on overall space on the image sensor. Gowda teaches an image sensor where pixels correspond to ADC, which in view of Pixel-Level Memory, corresponds to an AD memory, in a variety of relationships as taught in Col 2 Lines 39-44, "those skilled in the art will appreciate that the same function can be performed using any ADC architecture such as one per column, one per pixel, several per column, etc.".

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the teaching of Pixel-Level Memory with that of Gowda to realize that the two or more pixels can share an ADC, which corresponds to sharing an AD memory which performs the ADC. This would be obvious to save room overall on the sensor chip by reducing the number of components for some pixels.

7. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Pixel-Level Memory in view of Bell et al. (US 7106372).

Regarding Claim 7, Pixel-Level Memory teaches the solid-state imaging apparatus according to claim 1, and teaches simultaneous A/D conversion and discloses the signals are read from the pixel array to the AD memory, however does not teach that this is performed on a row by pixel row basis. Although Pixel-Level Memory teaches one ADC and AD memory for each pixel, which improves over row by row read out to AD memory, however it is well known and conventional for this process to be on a

row by row basis as taught by Bell in Col 4 Lines 55-60, where in the context of Pixel-Level Memory, the ADC is associated with the AD memory. One of ordinary skill in the art would realize the original method of the improved method of Pixel-Level Memory and would be motivated to read out the signals on a row to row basis to the AD memory for synchronization of timing with other aspects of the image sensor.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to AMY HSU whose telephone number is (571)270-3012. The examiner can normally be reached on M-F 8am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lin Ye can be reached on 571-272-7372. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Amy Hsu
Examiner
Art Unit 2622

ARH 11/4/08

/Lin Ye/
Supervisory Patent Examiner, Art Unit 2622